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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,928	12/08/2003	Yoshinori Kitamura	246239US2S	9664

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,928	KITAMURA ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-10 in the reply filed on 11/08/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda et al. (U.S. Pat. 6,403,421).

Regarding claim 1, Ikeda (figures 9A-11I) discloses a semiconductor device comprising:

a semiconductor substrate 10 including first and second element-formation regions which are partitioned by an isolation trench T (see figure 9C, column 13, lines 46-53);

first and second lower gate insulating films 20a formed on the first and second element-formation regions, respectively (see figure 9C, column 13, lines 24-25);

first and second floating gates 30a formed on the first and second lower gate insulating films 20, respectively (see figure 9C, column 13, lines 24-33);

an isolation insulating film 24, which is formed at least in the isolation trench T and which has a depression formed in an upper surface thereof (see figure 10E, column 14, lines 5-15);

an upper gate insulating film 25 formed on the first and second floating gates 33 (see figure 11I, column 14, lines 40-41); and

control gate line 31 including an opposed portion which is opposed to the first and second floating gates 33, with the upper gate insulating film 25 being interposed, and a portion located inside the depression (see figure 11I, column 14, lines 40-49),

the first floating gates 33 including a side surface which is opposed to the second floating gate 33 and which entirely aligns with a side surface included in the first element-formation region and defined by the isolation trench T, and the second floating gate 33 including a side surface which is opposed to the first floating gate and which entirely aligns with a side surface included in the second element-formation region and defined by the isolation trench T (see figure 11I).

Regarding claim 2, Ikeda (figure 10E) discloses wherein the isolation insulating film 24 includes an uppermost portion located higher than lower surfaces of the first and second floating gates 30a.

Regarding claim 3, Ikeda (figure 10F) discloses wherein the isolation insulating film 24a includes an uppermost portion located lower than upper surfaces the first and second floating gates 30a.

Regarding claim 4, Ikeda (figure 11I) discloses wherein the opposed portion of the control gate line 31 is opposed to the upper surfaces of the first and second floating gates 33 and is opposed to those portions of the side surfaces of the first and second floating gates 33 which are located higher than the uppermost portion the isolation insulating film 24a.

Regarding claim 5, Ikeda (figure 11I) discloses wherein the isolation insulating film 24a includes an uppermost portion located higher than lower surfaces of the first and second floating gates 33 and lower than upper surfaces of the first and second floating gates 33.

Regarding claim 6, Ikeda (figure 11I) discloses wherein the control gate line 31 includes a lowermost portion located lower than lower surfaces of the first and second floating gates 33.

Regarding claim 7, Ikeda (figure 11I) discloses the upper gate insulating film 25 includes a portion extended onto the isolation insulating film 24a.

Regarding claim 8, Ikeda (figure 6A) discloses wherein the depression filled with the control gate line 31a.

Regarding claim 9, Ikeda (figure 6B) discloses wherein the isolation insulating film 24a has a thickness smaller than a half of a width of the isolation trench T.

Regarding claim 10, Ikeda discloses wherein the isolation insulating film 24 formed by CVD (see figure 4C, column 4, lines 47-49). It is note that the process limitation (formed by CVD) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

4. Claims 1-4 and 6-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Aritome (U.S. Pat. 5,949,101) of record.

Regarding claim 1, Aritome (figures 9A-9E) discloses a semiconductor device comprising:

a semiconductor substrate 1B including first and second element-formation regions which are partitioned by an isolation trench 11 (see figure 9B, column 8, lines 43-60);

first and second lower gate insulating films 32 formed on the first and second element-formation regions, respectively (see figure 9C);

first and second floating gates 4 formed on the first and second lower gate insulating films 32, respectively (see figure 9D, column 8, lines 56-60 and column 9, lines 26-38);

an isolation insulating film 2, which is formed at least in the isolation trench 11 and which has a depression formed in an upper surface thereof (see figure 9C, column 9, lines 8-13);

an upper gate insulating film 33 formed on the first and second floating gates 4 (see figure 9D, column 9, lines 26-38); and

control gate line 6 including an opposed portion which is opposed to the first and second floating gates 4, with the upper gate insulating film 33 being interposed, and a portion located inside the depression (see figure 9D, column 9, lines 39-43),

the first floating gates 4 including a side surface which is opposed to the second floating gate and which entirely aligns with a side surface included in the first element-formation region and defined by the isolation trench 11, and the second floating gate including a side surface which is opposed to the first floating gate and which entirely aligns with a side surface included in the second element-formation region and defined by the isolation trench 11 (see figure 9E).

Regarding claim 2, Aritome discloses wherein the isolation insulating film 2 includes an uppermost portion located higher than lower surfaces of the first and second floating gates 4 (column 9, lines 8-17).

Regarding claim 3, Aritome (figure 9C) discloses wherein the isolation insulating film 2 includes an uppermost portion located lower than upper surfaces the first and second floating gates 4.

Regarding claim 4, Aritome (figure 9D) discloses wherein the opposed portion of the control gate line 6 is opposed to the upper surfaces of the first and second floating gates 4 and is opposed to those portions of the side surfaces of the first and second floating gates which are located higher than the uppermost portion the isolation insulating film 2.

Regarding claim 6, Aritome (figure 9D) discloses wherein the control gate line 6 includes a lowermost portion located lower than lower surfaces of the first and second floating gates 4.

Regarding claim 7, Aritome (figure 9D) discloses the upper gate insulating film 33 includes a portion extended onto the isolation insulating film 2.

Regarding claim 8, Aritome (figure 9D) discloses wherein the depression filled with the control gate line 6.

Regarding claim 9, Aritome (figure 9C) discloses wherein the isolation insulating film 2 has a thickness smaller than a half of a width of the isolation trench 11.

Regarding claim 10, Aritome discloses wherein the isolation insulating film 2 formed by CVD (see figure 9C, column 9, lines 8-10). It is note that the process

limitation (formed by CVD) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TD
January 31, 2005.

PHAT X. CAO
PRIMARY EXAMINER